**Amendments to the Claims**

This listing of claims will replace all prior version, and listings, of claims in the application.

**Listing of Claims:**

1. (previously presented) A multi-layer semiconductor chip package, comprising:

a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly,

wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

2. – 4. (canceled)

5. (previously presented) The package of claim 1, wherein the adjacent pairs of conductors are positioned orthogonally to each other.

6. (previously presented) The package of claim 1, wherein the adjacent pairs of conductors are positioned to be equidistant to each other.

7. (original) The package of claim 1, wherein the layer is near an interface between the carrier and a chip.

8. – 14. (canceled)

15. (previously presented) A connector capable of being coupled to a semiconductor chip package, comprising:

a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly,

wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

16. (canceled)

17. (previously presented) The connector of claim 15, wherein the adjacent pairs of conductors are positioned to be equidistant to each other.

18. (previously presented) A method for providing a semiconductor chip package, comprising the steps of:

(a) providing a plurality of pairs of conductors for carrying a plurality of signals in a layer of a carrier of the package, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly,

wherein cross-talk between the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

19. – 21. (canceled)

22. (previously presented) The method of claim 18, wherein the adjacent pairs of

conductors are positioned to be equidistant to each other.

23. (original) The method of claim 18, wherein the layer is near an interface between the carrier and a chip.